Technical Information Manual

Revision n. 12

06 February 2012

MOD. V1751

4/8 CH. 10BIT
2/1 GS/s DIGITIZER
MANUAL REV.12

NPO:
00105/08:V1751x.MUTx/12

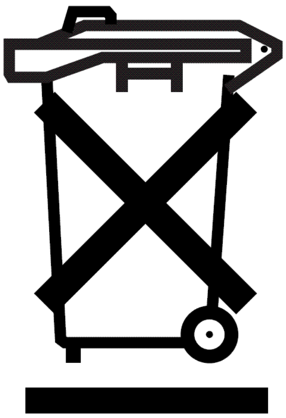
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1. General description

1.1. Overview

The Mod. V1751 is a 1-unit wide VME 6U module housing a 8 Channel 10 bit 1 GS/s Flash ADC Waveform Digitizer with threshold Auto-Trigger capabilities. The Mod. V1751 can work also as 4 Channel 10 bit 2 GS/s Flash ADC Waveform Digitizer (Dual Edge Sampling).

Input dynamics is 1 Vpp (single ended or differential).

The DC offset of the input signal can be adjusted channel per channel by a programmable 16bit DAC on single ended input version.

The module features a front panel clock/reference In/Out and a PLL for clock synthesis from internal/external references. This allows multi board phase synchronizations to an external clock reference or to a clock Digitizer master board.

The data stream is continuously written in a circular memory buffer. When the trigger occurs, the FPGA writes further N samples for the post trigger and freezes the buffer that can be read either via VME or via Optical Link. The acquisition can continue without dead time in a new buffer.

Each channel has a SRAM memory buffer (available in the 1.835 and 14.4 MSamples/ch sizes, which become 3.6 and 28.8 MSamples/ch when using Dual Edge Sampling), with independent read-write access divided in 1 to 1024 buffers of programmable size.

The trigger signal can be provided via the front panel input as well as via the VMEbus, but it can also be generated internally. The trigger from one board can be propagated to the other boards through the front panel Trigger Output.

An Analog Output allows to reproduce the trigger majority, a test waveform and the buffer occupancy.

The Modules VME interface is VME64X compliant and the data readout can be performed in Single Data Transfer (D32), 32/64 bit Block Transfer (BLT, MBLT, 2eVME, 2eSST) and 32/64 bit Chained Block Transfer (CBLT).

The boards houses a daisy chainable Optical Link able to transfer data at 80 MB/s, thus it is possible to connect up to eight ADC boards (64 ADC channels) to a single Optical Link Controller (Mod. A2818). Optical Link and VME access are internally arbitrated.

Table 1.1: Available items

Code	Model	Form factor	Input	Memory
WV1751XAAAAA	V1751	6U-VME64	Single ended	1.8/3.6MS/ch
WV1751BXAAAA	V1751B	6U-VME64	Differential	1.8/3.6MS/ch
WV1751CXAAAA	V1751C	6U-VME64	Single ended	14.4/28.8MS/ch
WVX1751XAAAA	VX1751	6U-VME64X	Single ended	1.8/3.6MS/ch
WVX1751BXAAA	VX1751B	6U-VME64X	Differential	1.8/3.6MS/ch
WVX1751CXAAA	VX1751C	6U-VME64X	Single ended	14.4/28.8MS/ch

1.2. Block Diagram

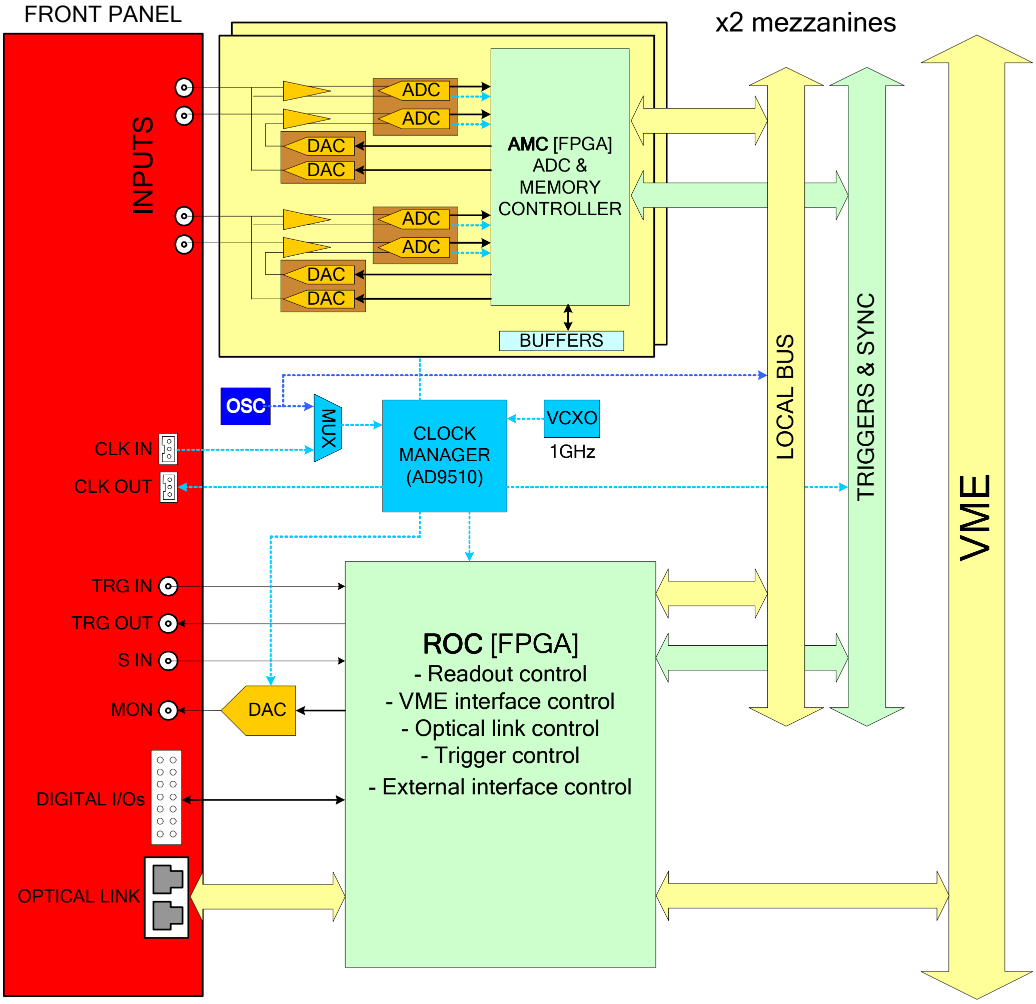


Fig. 1.1: Mod. V1751 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical specifications

2.1. Packaging and Compliancy

2.1.1. Supported VME Crates

The module is housed in a 6U-high, 1U-wide VME unit. The board hosts the VME P1, and P2 connectors and fits into both VME/VME64 standard and V430 backplanes.
VX1751 versions fit VME64X compliant crates.

2.2. Power requirements

The power requirements of the module are as follows:

Table 2.1: Model V1751 power requirements

+5 V	6.5A
+12 V	0.2A
-12 V	0.3A

2.3. Front Panel

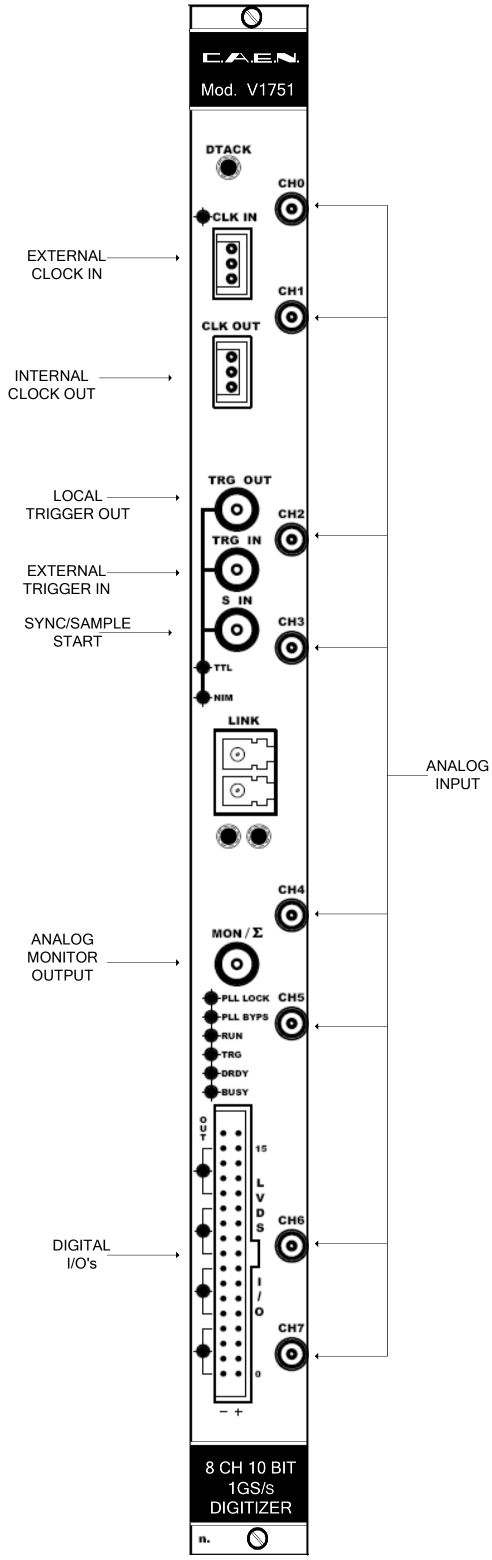


Fig. 2.1: Mod. V1751 front panel

2.4. External connectors

2.4.1. ANALOG INPUT connectors

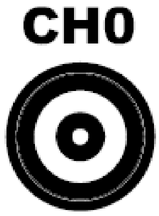


Fig. 2.2: MCX connector

Single ended version (see options in § 1.1):
Function:
Analog input, single ended, input dynamics: 1Vpp Zin=50Ω
Mechanical specifications:
MCX connector (CS 85MCX-50-0-16 SUHNER)
When Dual Edge Sampling mode is used, make sure that the EVEN channels are disconnected
Absolute max analog input voltage: 3Vpp (with Vrail max +3V or -3V) for any DAC offset in single ended configuration

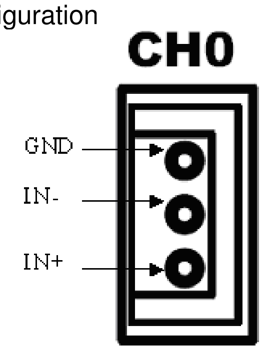


Fig. 2.3: AMP Differential connector

Differential version (see options in § 1.1):
Function:
Analog input, differential, input dynamics: 1Vpp Zin=100Ω
Mechanical specifications:
AMP 3-102203-4 AMP MODUII
Absolute max analog input voltage: T.B.D.
When Dual Edge Sampling mode is used, make sure that the EVEN channels are disconnected
Absolute max analog input voltage: 3Vpp (with Vrail max +3V or -3V) in differential configuration.

2.4.2. CONTROL connectors

Function:
- TRG OUT: Local trigger output (NIM/TTL, on Rt = 50Ω)
- TRG IN: External trigger input (NIM/TTL, Zin= 50Ω)
- SYNC/SAMPLE/START: Sample front panel input (NIM/TTL, Zin=50Ω)

- MON/Σ: DAC output 1Vpp on Rt=50Ω

Mechanical specifications:
00-type LEMO connectors

2.4.3. ADC REFERENCE CLOCK connectors

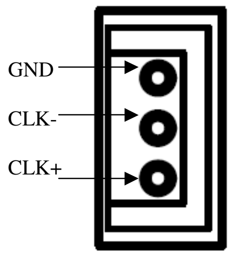


Fig. 2.4: AMP CLK IN/OUT Connector

Function:
CLK IN: External clock/Reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Zdiff= 100Ω.
Mechanical specifications:
AMP 3-102203-4 connector
Function:
CLOCK OUT: Clock output, DC coupled (diff. LVDS), Zdiff = 100Ω.
Mechanical specifications:
AMP 3-102203-4 connector

2.4.4. Digital I/O connectors

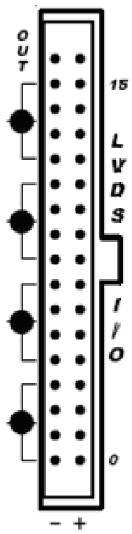


Fig. 2.5: Programmable IN/OUT Connector

Function: N.16 programmable differential LVDS I/O signals, Zdiff_in= 100Ω. Four Independent signal group 0÷3, 4÷7, 8÷11, 12÷15, In / Out direction control; see also § 3.5.
Mechanical specifications:
3M-7634-5002- 34 pin Header Connector

2.4.5. Optical LINK connector

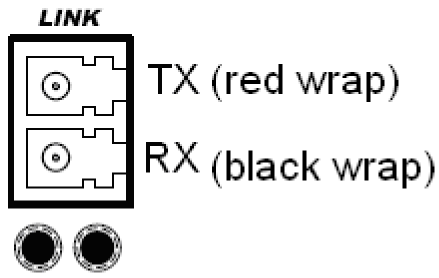


Fig. 2.6: LC Optical Connector

Mechanical specifications:
LC type connector; to be used with Multimode 62.5/125µm cable with LC connectors on both sides
Electrical specifications:
Optical link for data readout and slow control with transfer rate up to 80MB/s; daisy chainable.

2.5. Other front panel components

2.5.1. Displays

The front panel hosts the following LEDs:

Table 2.2: Front panel LEDs

Name:	Colour:	Function:
DTACK	green	VME read/write access to the board
CLK_IN	green	External clock enabled.
NIM	green	Standard selection for TRG OUT, TRG IN, S IN.
TTL	green	Standard selection for TRG OUT, TRG IN, S IN.
LINK	green/yellow	Network present; Data transfer activity
PLL _LOCK	green	The PLL is locked to the reference clock
PLL _BYPS	green	The reference clock drives directly ADC clocks; the PLL circuit is switched off and the PLL_LOCK LED is turned off.
RUN	green	RUN bit set (see § 5.18)
TRG	green	Triggers are accepted
DRDY	green	Event/data (depending on acquisition mode) are present in the Output Buffer
BUSY	red	All the buffers are full
OUT_LVDS	green	Signal group OUT direction enabled.

2.6. Internal components

SW2,4,5,6 "Base Addr. [31:16]": Type: 4 rotary switches
Function: Set the VME base address of the module.

SW3 "CLOCK SOURCE" Type: Dip Switch
Function: Select clock source (External or Internal)

SW1 "FW" Type: Dip Switch.

Function: it allows to select whether the “Standard” (STD) or the “Back up” (BKP) firmware must be loaded at power on; (default position: STD).

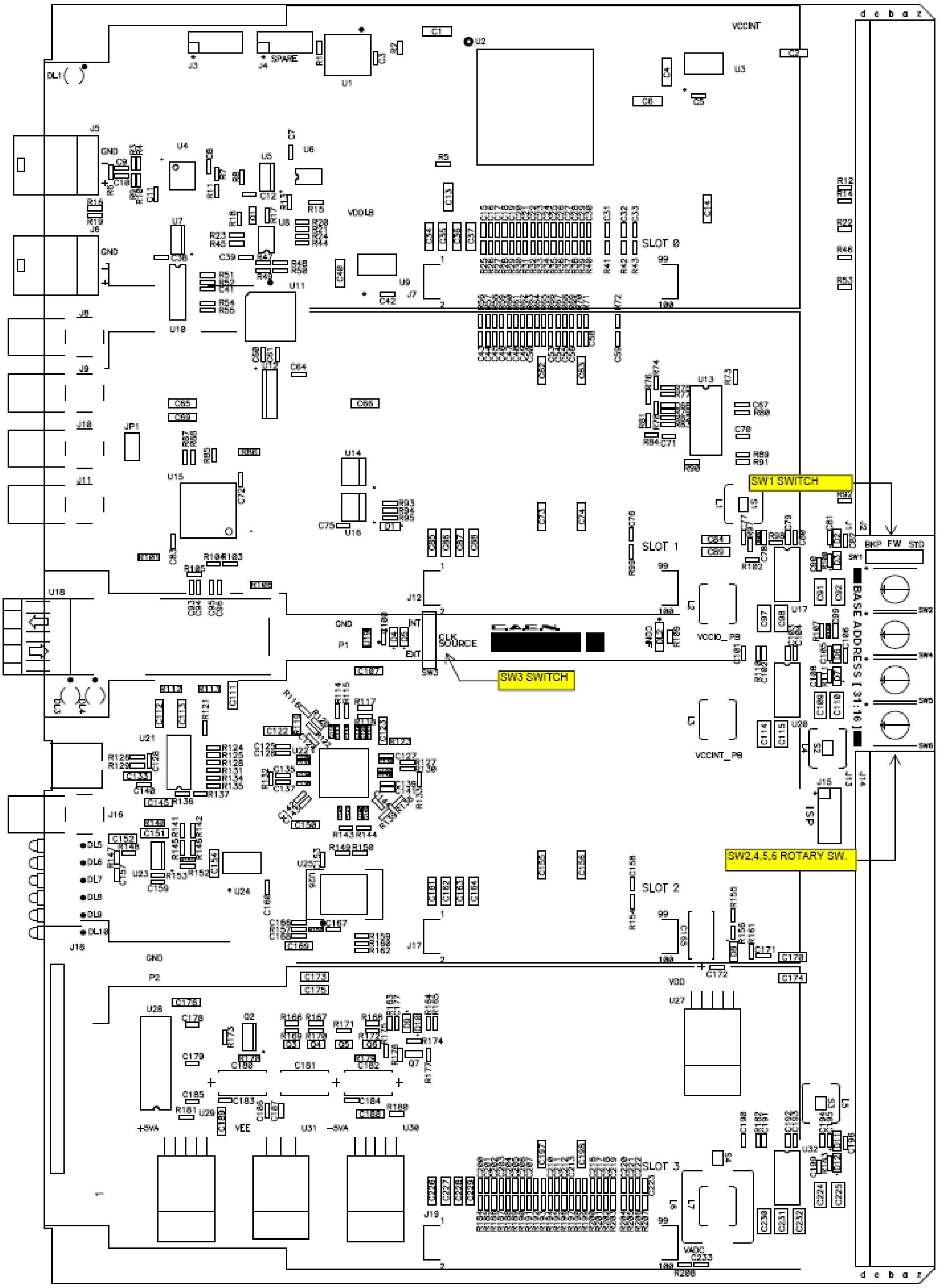


Fig. 2.7: Rotary and dip switches location

2.7. Technical specifications table

Table 2.3: Mod. V1751 technical specifications

Package	1-unit wide 6U-VME64 or 6U-VME64X module
Analog Input	8 channels, single-ended (SE) or differential. (4 channel in DES mode) Input range: 1Vpp; Bandwidth: 500MHz. Programmable DAC for Offset Adjust x ch. (SE only).
Digital Conversion	Resolution: 10 bit; Sampling rate: 1GS/s (2GS/s in DUAL EDGE SAMPLING mode) simultaneously on each channel; multi board synchronization (one board can act as clock master). External Gate Clock capability (NIM/TTL) for burst or single sampling mode.
ADC Sampling Clock generation	Three operating modes: - PLL mode - internal reference (50 MHz loc. oscillator). - PLL mode - external reference on CLK_IN (±100ppm tolerance). - PLL Bypass mode: Ext. 1GHz clock on CLK_IN drives directly ADC clocks for 1GS/s; 2GS/s in DUAL EDGE SAMPLING mode).
CLK_IN	AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available using cable adapter).
CLK_OUT	DC coupled differential LVDS output clock, locked to ADC sampling clock. Freq.: 10 ÷ 500MHz.
Memory Buffer	1.835 and 14.4 MSamples/ch sizes available (become 3.6 and 28.8 MSamples/ch in Dual Edge Sampling mode); Multi Event Buffer with independent read and write access. Programmable event size and pre-post trigger. Divisible into 1 ÷ 1024 buffers.
Trigger	Common External TRGIN (NIM or TTL) and VME Command Individual channel autotrigger (time over/under threshold)TRGOUT (NIM or TTL) for the trigger propagation to other boards.
Trigger Time Stamp	32bit – 4ns (34s range). Sync input for Time Stamp alignment
ADC and Memory controller FPGA	One FPGA Altera Cyclone EP3C16 for each ADC (2 channels)
Optical Link	Data readout and slow control with transfer rate up to 80 MB/s, to be used instead of VME bus. Daisy chainable: one A2818 PCI card can control and read eight boards in a chain.
VME interface	VME64X compliant D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast Cycles Transfer rate: 60MB/s (MBLT64), 100MB/s (2eVME), 160MB/s (2eSST). Sequential and random access to the data of the Multi Event Buffer. The Chained readout allows to read one event from all the boards in a VME crate with a BLT access.
Upgrade	V1751 firmware can be upgraded via VME or Optical Link
Software	General purpose C and LabVIEW Libraries; Demo and software tools for Windows and Linux
Analog Monitor	12bit / 125 MHz DAC FPGA controlled output, four operating modes: Test Waveform: 1 Vpp test ramp generator Majority: MON/Σ output signal is proportional to the number of channels (enabled) under/over threshold (1 step = 125mV) Buffer Occupancy: MON/Σ output signal is proportional to the Multi Event Buffer Occupancy Voltage level: MON/Σ output signal is a programmable voltage level
LVDS I/O	16 general purpose LVDS I/O controlled by the FPGA Busy, Data Ready, Memory full, Individual Trig-Out and other function can be programmed An Input Pattern from the LVDS I/O can be associated to each trigger as an event marker

3. Functional description

3.1. Analog Input

The module is available either with single ended (on MCX connector) or, on request, differential (on Tyco MODU II 3-pin connector) input channels.

3.1.1. Single ended input

Input dynamics is 1V (Zin= 50 Ω). 16bit DAC allow to add up to ±0.5V DC offset to preserve the full dynamic range also with unipolar positive or negative input signals. The input bandwidth ranges from DC to 500 MHz.

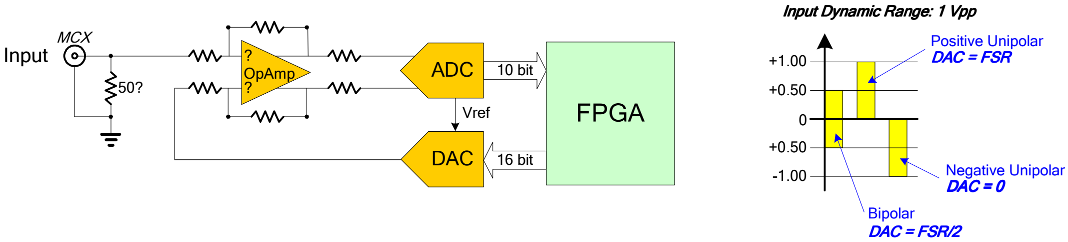


Fig. 3.1: Single ended input diagram

3.1.2. Differential input

Input dynamics is 1Vpp (Zdiff= 100 Ω).
The input bandwidth ranges from DC to 500 MHz.

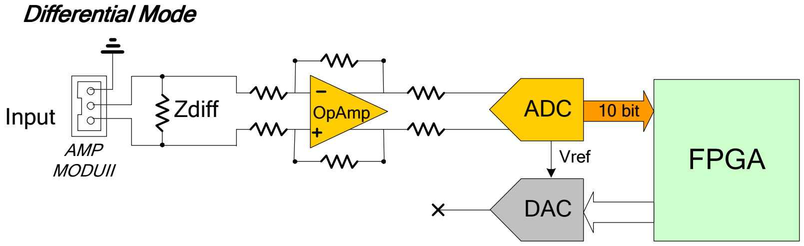


Fig. 3.2: Differential input diagram

3.2. Clock Distribution

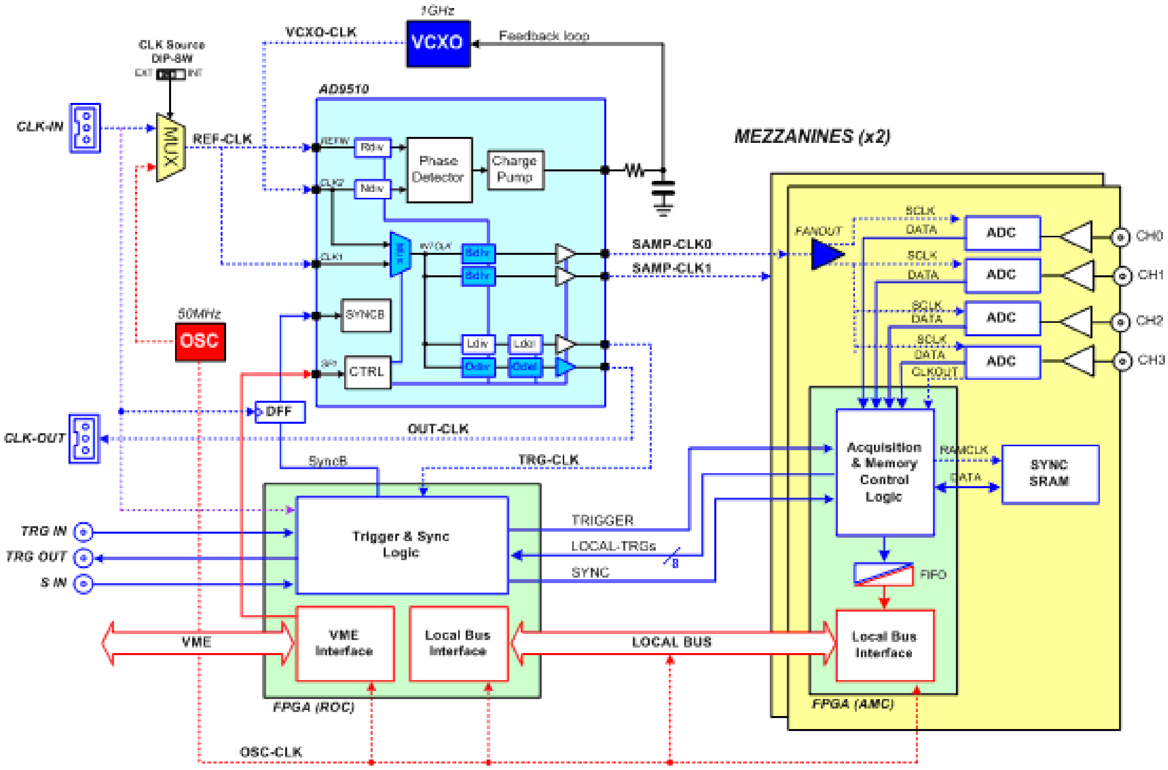


Fig. 3.3: Clock distribution diagram

The module clock distribution takes place on two domains: OSC-CLK and REF-CLK; the former is a fixed 50MHz clock provided by an on board oscillator, the latter provides the ADC sampling clock.
OSC-CLK handles both VME and Local Bus (communication between motherboard and mezzanine boards; see red traces in the figure above).
REF-CLK handles ADC sampling, trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source (selection is performed via dip switch SW1, see § 2.6); in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).
REF-CLK is processed by AD9510 device, which delivers 6 clock out signals; 4 signals are sent to ADCs, one to the trigger logic and one to drive CLK-OUT output (refer to AD9510 data sheet for more details:
http://www.analog.com/UploadedFiles/Data_Sheets/AD9510.pdf); two operating modes are foreseen: ***Direct Drive Mode*** and ***PLL Mode***

3.2.1. Direct Drive Mode

The aim of this mode is to drive externally the ADCs' Sampling Clock; generally this is necessary when the required sampling frequency is not a VCXO frequency sub multiple. The only requirement over the SAMP-CLK is to remain within the ADCs' range.

3.2.2. *PLL Mode*

The AD9510 features an internal Phase Detector which allows to couple REF-CLK with VCXO (1 GHz frequency); for this purpose it is necessary that REF-CLK is a sub multiple of 1 GHz.
AD9510 default setting foresees the board internal clock (50MHz) as clock source of REF-CLK.
This configuration leads to *Ndiv* = 100, *Rdiv* = 5, thus obtaining 10MHz at the Phase Detector input and CLK-INT = 1GHz.
The required 500 MHz Sampling Clock is obtained by processing CLK-INT through Sdiv dividers.
When an external clock source is used, if it has 50MHz frequency, then AD9510 programming is not necessary, otherwise Ndiv and Rdiv have to be modified in order to achieve PLL lock.
A REF-CLK frequency stability better than 100ppm is mandatory.

3.2.3. *Trigger Clock*

TRG-CLK signal has a frequency equal to 1/8 of SAMP-CLK; therefore a 8 samples “uncertainty” occurs over the acquisition window (16 samples uncertainty with V1751 operated at 2GS/s).

3.2.4. *Output Clock*

Front panel Clock Output is User programmable. Odiv and Odel parameters allows to obtain a signal with the desired frequency and phase shift (in order to recover cable line delay) and therefore to synchronize daisy chained boards. CLK-OUT default setting is OFF, it is necessary to enable the AD9510 output buffer to enable it.

3.2.5. *AD9510 programming*

CAEN has developed a software tool which allows to handle easily the clock parameters, the CAENupgrader; see www.caen.it path: Products / Front End / VME / Controller (VME)

3.2.6. PLL *programming*

In PLL mode the User has to enter the divider for input clock frequency (**input clock PLL mode,** via CAENupgrader); since the VCXO frequency is 1GHz, in order to use, for example, a 50MHz ExtClk, the divider to be entered is 20.
Then it is necessary to set the parameters for sampling clock and CLK_OUT (**enable**, **frequency** and **delay** in **Output Clock** field via CAENupgrader); the tool refuses wrong settings for such parameters.

3.2.7. Direct Drive *programming*

In Direct Drive/BYPASS mode, the User can directly set the input frequency (**Input Clock** field, real values are allowed). Given an input frequency, it is possible to set the parameters in order to provide the required signals.

3.2.8. *Configuration file*

Once all parameters are set, the tool allows to save the configuration file which includes all the AD9510 device settings (see CAENupgrader documentation). It is also possible to browse and load into the AD9510 device a pre existing configuration file (see CAENupgrader documentation). For this purpose it is not necessary the board power cycle.

3.2.9. *Multiboard synchronization*

To be implemented.

3.3. Acquisition Modes

3.3.1. *Channel calibration*

In order to achieve best performance, a self channel calibration procedure should be run after the ADCs have stabilized their operating temperature. Whenever the operating temperature changes significantly, a new calibration procedure should be performed.
The calibration is performed through a write access to either Broadcast ADC Configuration or Channel n ADC Configuration register (see § 5.8 and 5.16); in order to achieve the best performance, it is strongly suggested to calibrate the channels through the Broadcast ADC Configuration register.

3.3.1.1. Normal mode self calibration

- Set to 0 the Calibration bit of Broadcast ADC Configuration register.
- Set such bit to 1. The self calibration process will start and the flag "Calibrating bit" of Channel n Status register (see § 5.4) will be set to 0.
- Polling on the flag "Calibrating bit" until it returns to 1 (few milliseconds).
- Set again to 0 the Calibration bit of Broadcast ADC Configuration register

3.3.1.2. Dual Edge Sampling mode self calibration

- Make sure that the EVEN channels are <u>disconnected</u>
- Disable (mask) EVEN channels (see § 5.25)
- Select Dual Edge Sampling mode (bit 12 of the channel configuration register, see § 5.9)
- Set to 0 the Calibration bit of Broadcast ADC Configuration register.
- Set such bit to 1. The self calibration process will start and the flag "Calibrating bit" of Channel n Status register (see § 5.4) will be set to 0.
- Polling on the flag "Calibrating bit" until it returns to 1 (few milliseconds).
- Set again to 0 the Calibration bit of Broadcast ADC Configuration register

Whenever switching from one mode (Normal or Dual Edge Sampling) to another, calibration must be repeated.

3.3.2. *Acquisition run/stop*

The acquisition can be started in two ways, according to Acquisition Control register Bits [1:0] setting (see § 5.16):

- setting the RUN/STOP bit (bit[2]) in the Acquisition Control register (bits [1:0] of Acquisition Control must be set to REGISTER-CONTROLLED RUN MODE or S-IN CONTROLLED RUN MODE)
- driving S_IN signal high (bits [1:0] of Acquisition Control must be set to 01)

Then acquisition is stopped either:

- resetting the RUN/STOP bit (bit[2]) in the Acquisition Control register (bits [1:0] of Acquisition Control must be set to REGISTER-CONTROLLED RUN MODE or S-IN CONTROLLED RUN MODE)
- driving S_IN signal low (bits [1:0] of Acquisition Control set to 01)

3.3.3. Acquisition Triggering: Samples and Events

When the acquisition is running, a trigger signal allows to:

- store the 32 bit counter (represents a time reference) of the Trigger Time Tag (TTT), that runs at 1/8 of the sampling clock frequency (1/16 with DES mode); actually the capture of the trigger takes place every 2 clock cycles, thus the time resolution of the Trigger Time Tag is 2 clock cycles (16 ns). This means that the LSB of the TTT is always 0.
- increment the EVENT COUNTER (see § 5.27)
- fill the active buffer with the pre/post-trigger samples, whose number is programmable (Acquisition window width, § 5.22), freezing then the buffer for readout purposes, while acquisition continues on another buffer

Table 3.1: Buffer Organization (case of 1.835Msample/ch memory)

REGISTER (see § 5.13)	BUFFER NUMBER	SIZE of one BUFFER (samples)	
		SRAM @ 1 GS/s	SRAM @ 2 GS/s
0x00	1	1.75M	3.5M
0x01	2	896k	1.75M
0x02	4	448k	896k
0x03	8	224k	448k
0x04	16	112k	224k
0x05	32	56k	112k
0x06	64	28k	56k
0x07	128	14k	28k
0x08	256	7k	14k
0x09	512	3584	7k
0x0A	1024	1792	3584

An event is therefore composed by the trigger time tag, pre- and post-trigger samples and the event counter.
Overlap between "acquisition windows" may occur (a new trigger occurs while the board is still storing the samples related to the previous trigger); this overlap can be either rejected or accepted (programmable via VME).
If the board is programmed to accept the overlapped triggers, as the "overlapping" trigger arrives, the current active buffer is filled up, then the samples storage continues on the subsequent one.
In this case events will not have all the same size (see figure below).

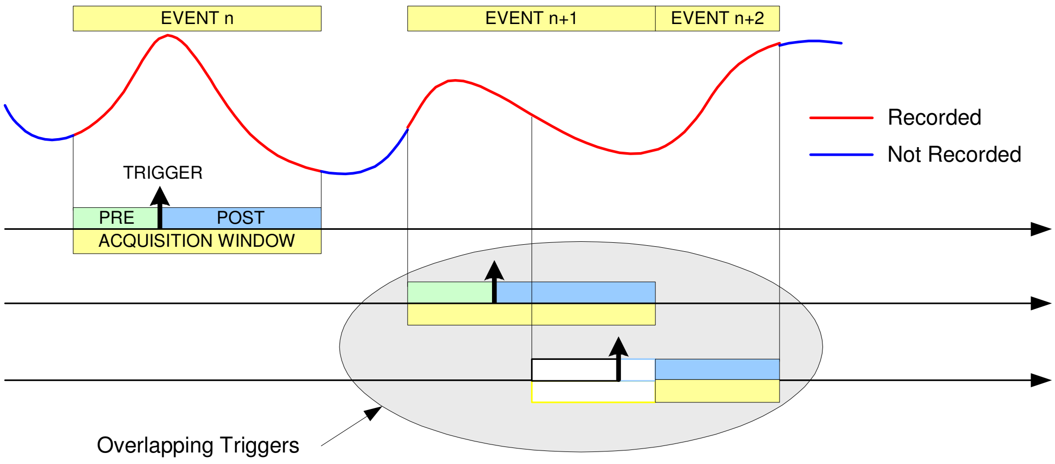


Fig. 3.4: Trigger Overlap

A trigger can be refused for the following causes:

- acquisition is not active
- memory is FULL and therefore there are no available buffers
- the required number of samples for building the pre-trigger of the event is not reached yet; this happens typically as the trigger occurs too early either with respect to the RUN_ACQUISITION command (see § 3.3.1) or with respect to a buffer emptying after a MEMORY_FULL status
- the trigger overlaps the previous one and the board is not enabled for accepting overlapped triggers

As a trigger is refused, the current buffer is not frozen and the acquisition continues writing on it. The Event Counter can be programmed in order to be either incremented or not. If this function is enabled, the Event Counter value identifies the number of the triggers sent (but the event number sequence is lost); if the function is not enabled, the Event Counter value coincides with the sequence of buffers saved and readout.

3.3.3.1. Custom size events

It is possible to make events with a number of Memory locations, which depends on Buffer Organization register setting (see § 5.13) smaller than the default value. One memory location contains 7 ADC samples and the maximum number of memory locations N_{LOC} is NS = 256K/Nblocks and NS = 2M/Nblocks, for 1.835 MSamples/ch and 14.4 MSamples/ch version respectively.
Smaller N_{LOC} values can be achieved by writing the number of locations N_{LOC} into the Custom Size register (see § 5.15).
N_{LOC} = 0 means “default size events”, i.e. the number of memory locations is the maximum allowed.
N_{LOC} = N1means that one event will be made of 7*N1 or 14*N1 (DES mode).

3.3.4. Event structure

An event is structured as follows:

- Header (4 32-bit words)
- Data (variable size)

The event can be readout either via VME or Optical Link; data format is 32 bit long word.

3.3.4.1. Header

It is composed by four words, namely:

- Size of the event (number of 32 bit long words)
- Board ID (GEO); Bit24; data format: 0; 16 bit pattern, latched on the LVDS I/O as one trigger arrives (see § 5.24); Channel Mask (=1: channels participating to event; ex CH5 and CH7 participating → Ch Mask: 0xA0, this information must be used by the software to acknowledge which channel the samples are coming from)
- Event Counter: It is the trigger counter; it can count either accepted triggers only, or all triggers (see § 5.15).
- Trigger Time Tag: It is a 32 bit counter (31 bit count + 1 overflow bit), which is reset either as acquisition starts or via front panel Reset signal (see § 3.8), and is incremented at each sampling clock hit. It is the trigger time reference.

3.3.4.2. Samples

Stored samples; data from masked channels are not read. When operating V1751 at 2 GS/s, "EVEN" channels are automatically disabled. Bit [31,30] are useful to acknowledge how many samples are in the last word of an event (1 to 3); example in § 3.3.4.3. shows a case with two samples in the last word.

3.3.4.3. Event format example

The event format is shown in the following figure (case of 8 channels enabled):

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td colspan="28">Event size</td><td rowspan="4">Header</td></tr>
<tr><td colspan="5">Board ID</td><td colspan="2">RES</td><td>0</td><td colspan="16">Pattern</td><td colspan="8">Channel mask</td></tr>
<tr><td colspan="8">Reserved</td><td colspan="24">Event counter</td></tr>
<tr><td colspan="32">Trigger time tag</td></tr>
<tr><td>1</td><td>1</td><td colspan="10">Sample 2 ch 0</td><td colspan="10">Sample 1 ch 0</td><td colspan="10">Sample 0 ch 0</td><td rowspan="4">Data ch 0</td></tr>
<tr><td>1</td><td>1</td><td colspan="10">Sample 5 ch 0</td><td colspan="10">Sample 4 ch 0</td><td colspan="10">Sample 3 ch 0</td></tr>
<tr><td colspan="32">...</td></tr>
<tr><td>1</td><td>0</td><td colspan="10"></td><td colspan="10">Sample n-1 ch 0</td><td colspan="10">Sample n-2 ch 0</td></tr>
<tr><td>1</td><td>1</td><td colspan="10">Sample 2 ch 1</td><td colspan="10">Sample 1 ch 1</td><td colspan="10">Sample 0 ch 1</td><td rowspan="4">Data ch 1</td></tr>
<tr><td>1</td><td>1</td><td colspan="10">Sample 5 ch 1</td><td colspan="10">Sample 4 ch 1</td><td colspan="10">Sample 3 ch 1</td></tr>
<tr><td colspan="32">...</td></tr>
<tr><td>1</td><td>0</td><td colspan="10"></td><td colspan="10">Sample n-1 ch 1</td><td colspan="10">Sample n-2 ch 1</td></tr>
<tr><td colspan="32">...</td><td></td></tr>
<tr><td>1</td><td>1</td><td colspan="10">Sample 2 ch 7</td><td colspan="10">Sample 1 ch 7</td><td colspan="10">Sample 0 ch 7</td><td rowspan="4">Data ch 7</td></tr>
<tr><td>1</td><td>1</td><td colspan="10">Sample 5 ch 7</td><td colspan="10">Sample 4 ch 7</td><td colspan="10">Sample 3 ch 7</td></tr>
<tr><td colspan="32">...</td></tr>
<tr><td>1</td><td>0</td><td colspan="10"></td><td colspan="10">Sample n-1 ch 7</td><td colspan="10">Sample n-2 ch 7</td></tr>
</table>

Fig. 3.5: Event Organization

3.3.5. Temperature monitor and power down

3.3.5.1. ADC chips temperature readout

The V1751 provide a ADC core temperature monitoring feature, useful in order to estimate the steady thermal state and to perform the calibration procedure (see § 3.3.1). Each ADC houses two channels (0-1, 2-3. 4-5, 6-7) so such registers provide identical temperature values in pairs; such values can be readout in the Channel n Temperature Monitor register (see § 5.9).

3.3.5.2. ADC chips over temperature protection

The V1751 provide an ADC thermal protection feature. Each ADC will be automatically powered off whenever the core temperature reaches 90°C. The relevant channels will not therefore participate any more to data event, and the OverTemp and PowerDown bits of Channel n Status register (see § 5.4) will set to 1.

When the ADC core temperature decreases under 65°C, the Over temperature flag of Channel n Status register will return to 0, and the relevant channels can be restored to normal operation following these steps:

- Wait until Over temperature flag (bit 8 of Channel n Status) register returns to 0
- Set to 0 Power Down configuration (bit 0 of Channel n ADC Configuration, see § 5.8)
  - Power Down flag (Bit 7 of Channel n Status register) will return to 0.
- Perform a calibration procedure on the restored channels (see § 3.3.1)
- Perform a channel synchronization (see § 5.29)

3.4. Trigger management

All the channels in a board share the same trigger: this means that all the channels store an event at the same time and in the same way (same number of samples and same position with respect to the trigger); several trigger sources are available.

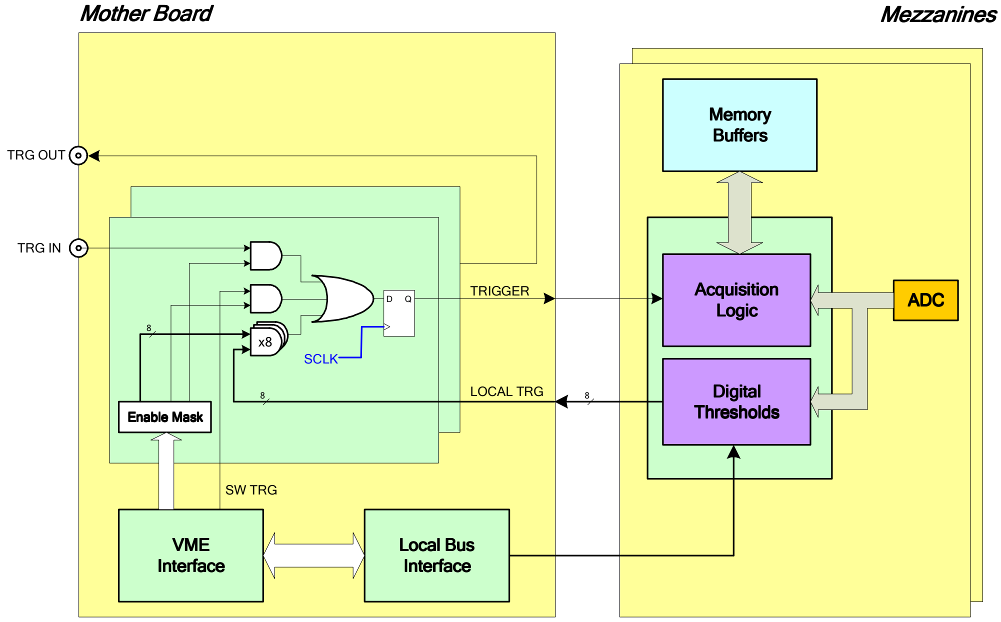


Fig. 3.6: Block diagram of Trigger management

3.4.1. External trigger

External trigger can be NIM/TTL signal on LEMO front panel connector, 50 Ohm impedance. The external trigger is synchronized with the internal clock (see § 3.2); if External trigger is not synchronized with the internal clock, a one clock period jitter occurs.

3.4.2. Software trigger

Software trigger are generated via VME bus (write access in the relevant register, see § 5.19).

3.4.3. Local channel auto-trigger

Each channel can generate a local trigger as the digitized signal exceeds the Vth threshold (ramping up or down, depending on Channel Configuration settings see § 5.9). The Vth digital threshold, the edge type are programmable via VME register accesses, see § 5.3.

N.B.: the local trigger signal does not start directly the event acquisition on the relevant channel; such signal is propagated to the central logic which produces the global trigger, which is distributed to all channels (see § 3.4.4).

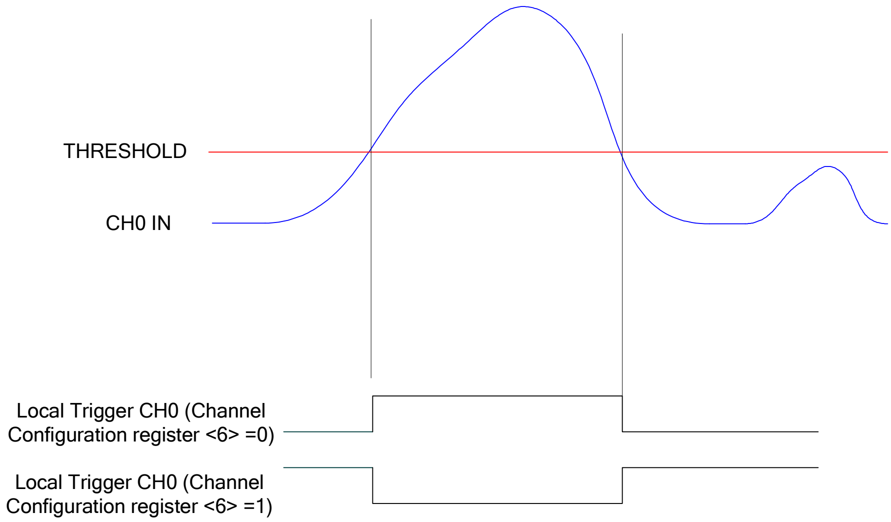


Fig. 3.7: Local trigger generation

3.4.3.1. Trigger coincidence level

It is possible to set the minimum number of channels that must be over threshold, beyond the triggering channel, in order to actually generate the local trigger signal. If, for example, Trigger Source Enable Mask (see § 0) bits[7:0]=FF (all channels enabled) and Local trigger coincidence level = 1 (bits [26:24]), whenever an enabled channel exceeds the threshold, the trigger will be generated only if at least another channel is over threshold at that moment. Local trigger coincidence level must be smaller than the number of channels enabled via bit[7:0] mask. The following figure shows examples with Local trigger coincidence level = 1 and = 0.

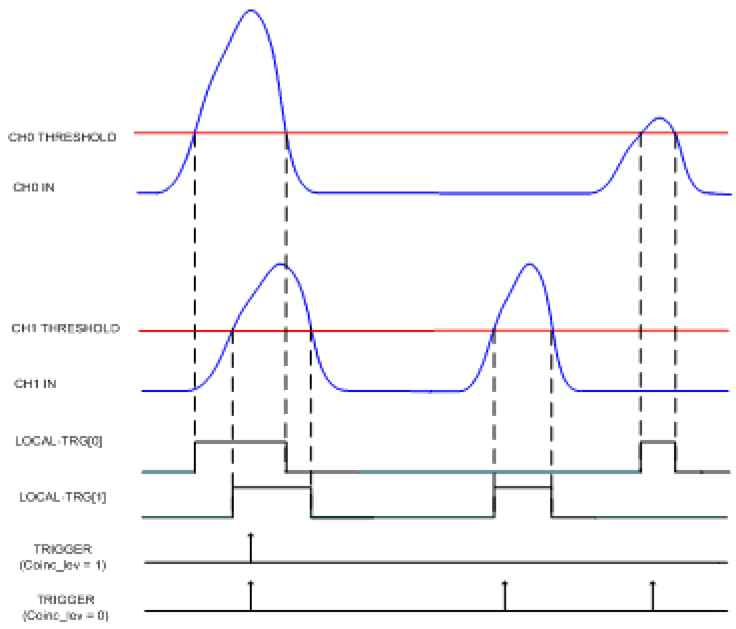


Fig. 3.8: Local trigger relationship with Coincidence level

3.4.4. Trigger distribution

The OR of all the enabled trigger sources, after being synchronized with the internal clock, becomes the global trigger of the board and is fed in parallel to all the channels, which store an event.
A Trigger Out is also generated on the relevant front panel TRG_OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards.
For example, in order to start the acquisition on all the channels in the crate, as one of the channels ramps over threshold, the Local Trigger must be enabled as Trigger Out, the Trigger Out must then be fed to a Fan Out unit; the obtained signal has to be fed to the External Trigger Input of all the boards in the crate (including the board which generated the Trigger Out signal).

3.5. Front Panel I/Os

The V1751 is provided with 16 programmable general purpose LVDS I/O signals. Signals can be programmed via VME (see § 5.23 and § 5.24).
Default configuration is:

Table 3.2: Front Panel I/Os default setting

Nr.	Direction	Description
0	out	Ch 0 Trigger Request
1	out	Ch 1 Trigger Request
2	out	Ch 2 Trigger Request
3	out	Ch 3 Trigger Request
4	out	Ch 4 Trigger Request
5	out	Ch 5 Trigger Request
6	out	Ch 6 Trigger Request

Nr.	Direction	Description
7	out	Ch 7 Trigger Request
8	out	Memory Full
9	out	Event Data Ready
10	out	Channels Trigger
11	out	RUN Status
12	in	Trigger Time Tag Reset (active low)
13	in	Memory Clear (active low)
14	-	RESERVED
15	-	RESERVED

3.6. Analog Monitor

The board houses a 12bit (125MHz) DAC with 0÷1 V dynamics on a 50 Ohm load (see Fig. 1.1), whose input is controlled by the ROC FPGA and the signal output (driving 50 Ohm) is available on the MON/Σ output connector. MON output of more boards can be summed by an external Linear Fan In.
This output is delivered by a 12 bit DAC.

The DAC control logic implements four operating modes:
- Trigger Majority Mode (Monitor Mode = 0)
- Test Mode (Monitor Mode = 1)
- Buffer Occupancy Mode (Monitor Mode = 3)
- Voltage Level Mode (Monitor Mode = 4)

Operating mode is selected via Monitor Mode register (see § 5.31); Monitor Mode = 2 is reserved for future implementation.

3.6.1. Trigger Majority Mode (Monitor Mode = 0)

It is possible to generate a Majority signal with the DAC: a voltage signal whose amplitude is proportional to the number of channels under/over (see § 5.3) threshold (1 step = 125mV); this allows, via an external discriminator, to produce a global trigger signal, as the number of triggering channels has exceeded a particular threshold.

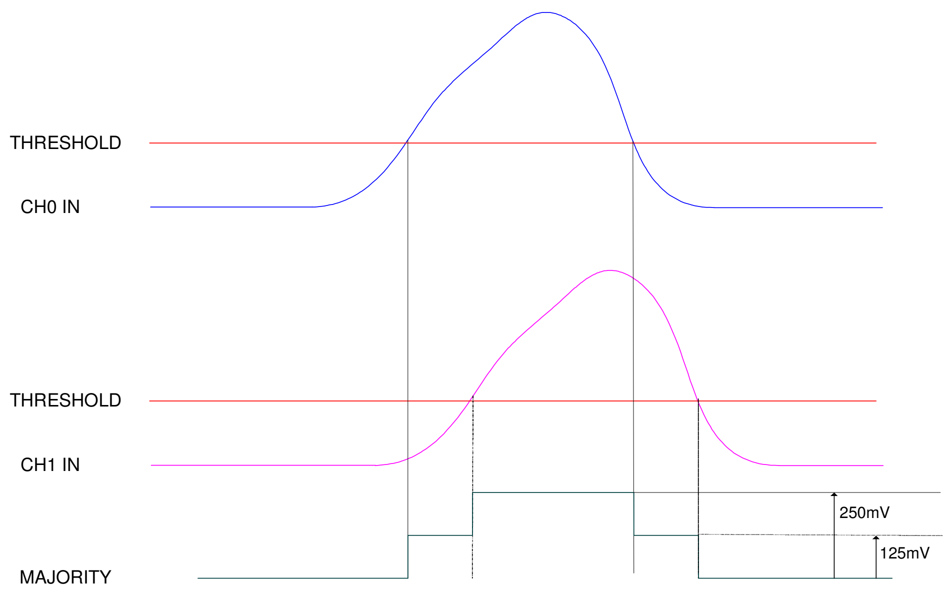


Fig. 3.9: Majority logic (2 channels over threshold; bit[6] of Ch. Config. Register =0)

In this mode the MON output provides a signal whose amplitude is proportional to the number of channels over the trigger threshold. The amplitude step (= +1 channel over threshold) is 125mV.

3.6.2. Test Mode (Monitor Mode = 1)

In this mode the MON output provides a sawtooth signal with 1 V amplitude and 30.518 Hz frequency.

3.6.3. Buffer Occupancy Mode (Monitor Mode = 3)

In this mode, MON out provides a voltage value proportional to the number of buffers filled with events; step: 1 buffer = 0.976 mV.
This mode allows to test the readout efficiency: in fact if the average event readout throughput is as fast as trigger rate, then MON out value remains constant; otherwise if MON out value grows in time, this means that readout rate is slower than trigger rate.

3.6.4. Voltage Level Mode (Monitor Mode = 4)

In this mode, MON out provides a voltage value programmable via the 'N' parameter written in the SET MONITOR DAC register, with: Vmon = 1/4096*N (Volt).

3.7. Test pattern generator

The FPGA AMC can emulate the ADC and write into memory a sawtooth signal for test purposes. It can be enabled via Channel Configuration register, see § 5.9.
The following figure shows the test ramps for even and odd channels respectively.

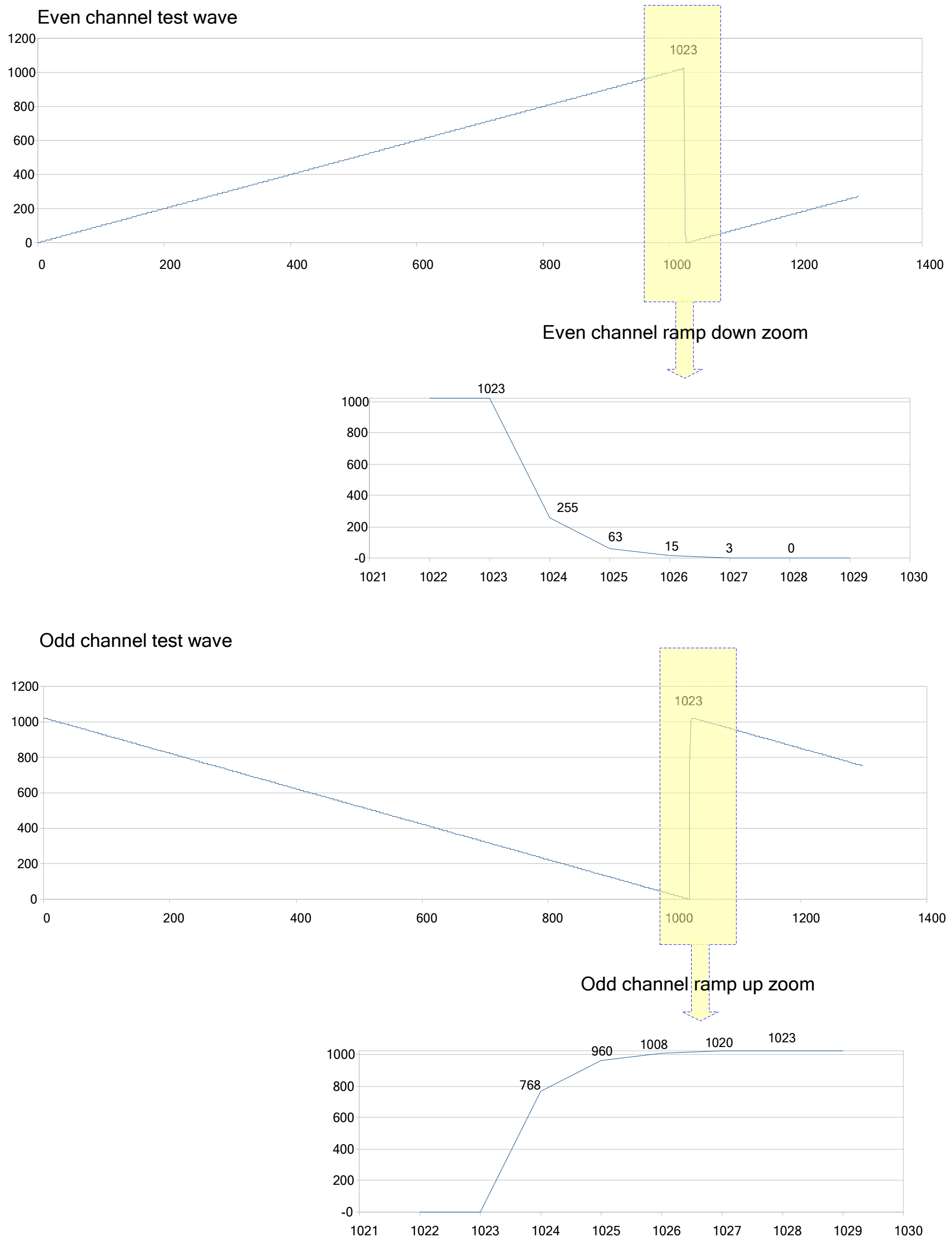


Fig. 3.10: FPGA test waveform

3.8. Reset, Clear and Default Configuration

3.8.1. Global Reset

Global Reset is performed:

- at Power ON of the module
- via a VME RESET (SYSRES)
- Software reset (see § 5.42)

It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

3.8.2. Memory Reset

The Memory Reset clears the data off the Output Buffer.
The Memory Reset can be forwarded via either a write access to Software Clear Register (see § 5.43) or with a pulse sent to the front panel Memory Clear input (see § 3.5).

3.8.3. Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to Trigger Time Tag Reset input (see § 3.5).

3.9. VMEbus interface

The module is provided with a fully compliant VME64/VME64X interface (see § 1.1), whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA/ROAK interrupter
- Configuration ROM

3.9.1. Addressing capabilities

3.9.1.1. Base address

The module works in A24/A32 mode. The Base Address of the module can be fixed through four rotary switches (see § 2.6) and is written into a word of 24 or 32 bit.
The Base Address can be selected in the range:

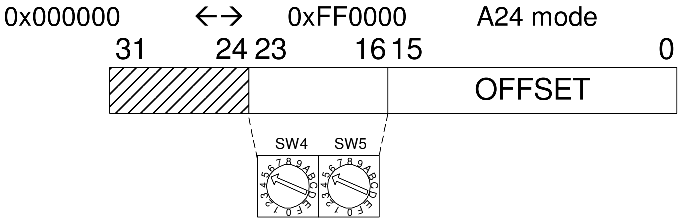


Fig. 3.11: A24 addressing

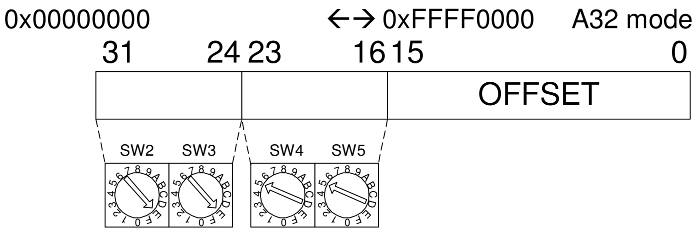


Fig. 3.12: A32 addressing

The Base Address of the module is selected through four rotary switches (see § 2.6), then it is validated only with either a Power ON cycle or a System Reset (see § 3.8).

3.9.1.2. CR/CSR address

GEO address is picked up from relevant backplane lines and written onto bit 23..19 of CR/CSR space, indicating the slot number in the crate; the recognized Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160pin connectors*.

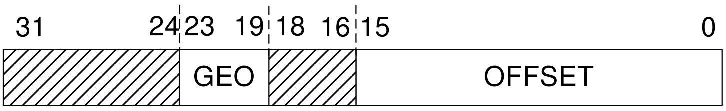


Fig. 3.13: CR/CSR addressing

3.9.1.3. Address relocation

Relocation Address register (see § 5.37) allows to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via VME Control Register (see § 5.28). The used addresses are:

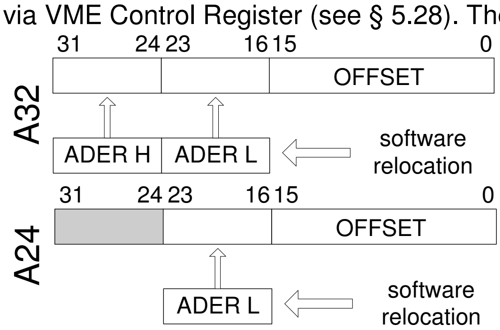


Fig. 3.14: Software relocation of base address

3.10. Data transfer capabilities

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

3.11. Events readout

3.11.1. Sequential readout

The events, once written in the SRAMs (Memory Event Buffers), become available for readout via VME. During the memory readout, the board can continue to store more events (independently from the readout) on the free buffers. The acquisition process is therefore "deadtimeless", until the memory becomes full.
Although the memories are SRAMs, VMEBus does not handle directly the addresses, but takes them from a FIFO. Therefore, data are read from the memories sequentially, according to the selected Readout Logic, from a memory space mapped on 4Kbytes (0x0000÷0x0FFC).
The events are readout sequentially and completely, starting from the Header of the first available event, followed by the Trigger Time Tag, the Event Counter and all the samples of the channels (from 0 to 7). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially (see also § 3.3.4).

3.11.1.1. SINGLE D32

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § 3.3.4.
We suggest, after the 1st word is transferred, to check the Event Size information and then do as many D32 cycles as necessary (actually Event Size -1) in order to read completely the event.

3.11.1.2. BLOCK TRANSFER D32/D64, 2eVME

BLT32 allows, via a single channel access, to read N events in sequence, N is set via the BLT Event Number register (see § 5.40).
The event size depends on the Buffer Size Register setting (§ 5.13); namely:

```
[Event Size] = [8*(Block Size)] + [16 bytes]
```

Then it is necessary to perform as many cycles as required in order to readout the programmed number of events.
We suggest to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

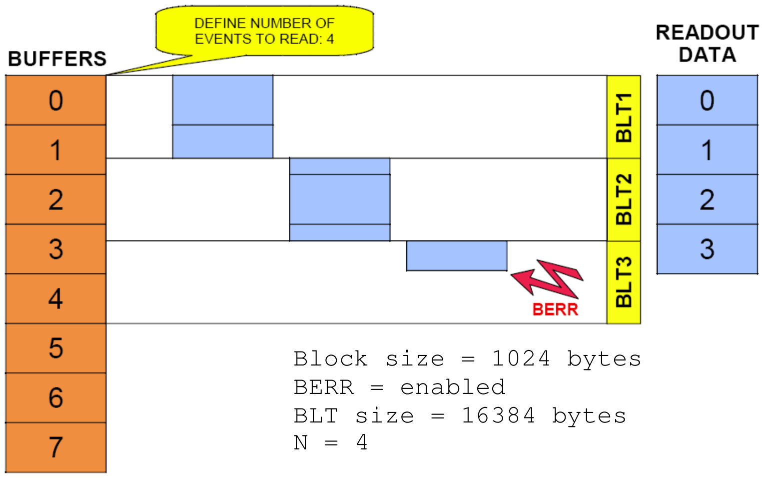


Fig. 3.15: Example of BLT readout

Since some 64 bit CPU's cut off the last 32 bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit in the VME Control register (see § 5.28).

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

3.11.1.3. CHAINED BLOCK TRANSFER D32/D64

The V1751 allows to readout events from more daisy chained boards (Chained Block Transfer mode).
The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles.
Several contiguous boards, in order to be daisy chained, must be configured as "first", "intermediate" or "last" via MCST Base Address and Control Register (see § 5.36). A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the "first" board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the "last" board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.
If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

3.11.2. Random readout (to be implemented)

Events can be readout partially (not necessarily starting from the first available) and are not erased from the memories, unless a command is performed. In order to perform the random readout it is necessary to execute an ***Event Block Request*** via VME.
Indicating the event to be read (page number = 12 bit datum), the offset of the first word to be read inside the event (12 bit datum) and the number of words to be read (size = 10 bit datum). At this point the data space can be read, starting from the header (which

reports the required size, not the actual one, of the event), the Trigger Time Tag, the Event Counter and the part of the event required on the channel addressed in the Event Block Request.
After data readout, in order to perform a new random readout, it is necessary a new Event Block Request, otherwise Bus Error is signaled. In order to empty the buffers, it is necessary a write access to the Buffer Free register (see § 5.14): the datum written is the number of buffers in sequence to be emptied.

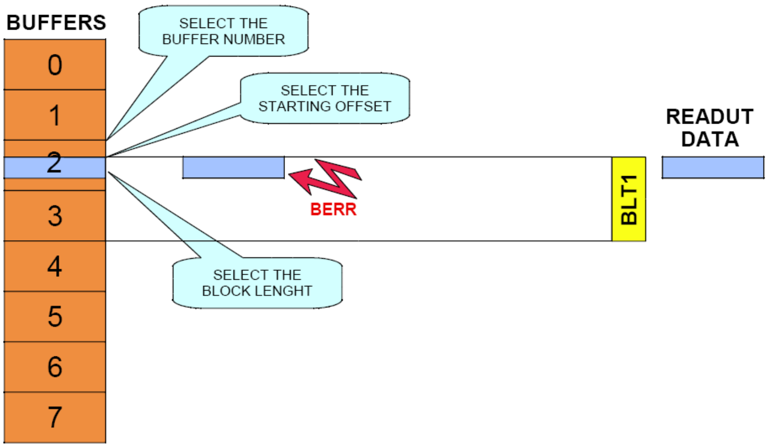


Fig. 3.16: Example of random readout

3.12. Optical Link

The board houses a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight V1751 to a single Optical Link Controller: for more information, see www.caen.it (path: Products / Front End / PCI/PCIe / Optical Controller)
The parameters for read/write accesses via optical link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.
VME Control Register bit 3 allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.
VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

4. Software tools

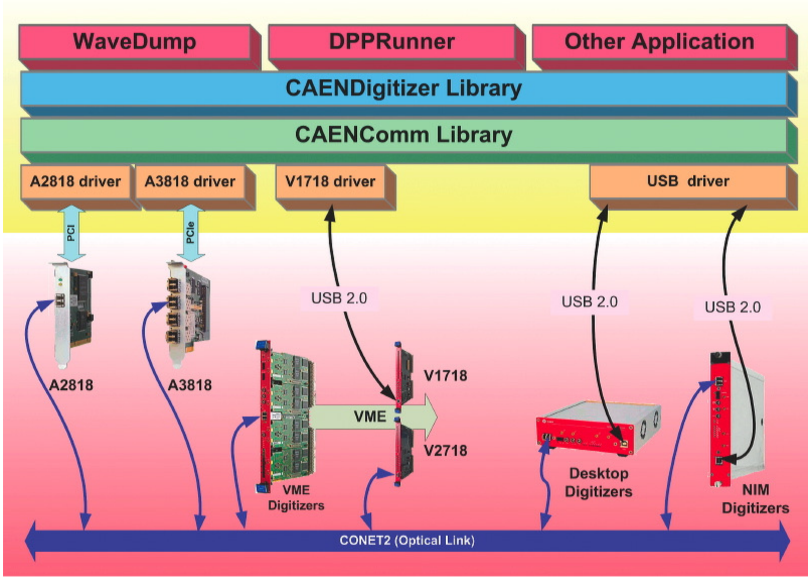


Fig. 4.1: Block diagram of the software layers

CAEN provides drivers for both the physical communication channels (the proprietary CONET Optical Link managed by the A2818 PCI card or A3818 PCIe cards and the VME bus accessed by the V1718 and V2718 bridges; refer to the related User Manuals), a set of C and LabView libraries, demo applications and utilities. Windows and Linux are both supported. The available software is the following:

- **CAENComm** library contains the basic functions for access to hardware; the aim of this library is to provide a unique interface to the higher layers regardless the type of physical communication channel. Note: for VME access, CAENcomm is based on CAEN's VME bridges V1718 (USB to VME) and V2718 (PCI/PCIe to VME). In the case of third-part bridges or SBCs, the user must provide the functions contained in the CAENcomm library for the relevant platform. The CAENComm requires the CAENVMELib library to be installed even in the cases where the VME is not used.
- **CAENDigitizer** is a library of functions designed specifically for the digitizer family and it supports also the boards running special DPP (Digital Pulse Processing) firmware. The purpose of this library is to allow the user to open the digitizer, program it and manage the data acquisition in an easy way: with few lines of code the user can make a simple readout program without the necessity to know the details of the registers and the event data format. The CAENDigitizer library implements a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENDigitizer independent from the physical layer. The library is based on the CAENComm library that manages the communication at low level (read and write access). CAENVMELib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer; however, both CAENVMELib and CAENComm libraries are completely transparent to the user.
- **WaveDump** is a Console application that allows to program the digitizer (according to a text configuration file that contains a list of parameters and instructions), to start the acquisition, read the data, display the readout and trigger rate, apply some post processing (such as FFT and amplitude histogram), save data to a file and also plot

the waveforms using the external plotting tool "gnuplot", available on internet for free. This program is quite basic and has no graphics but it is an excellent example of C code that demonstrates the use of libraries and methods for an efficient readout and data analysis. **NOTE:** WaveDump does not work with digitizers running DPP firmware. The users who intend to write the software on their own are suggested to start with this demo and modify it according to their needs. For more details please see the WaveDump User Manual and Quick Start Guide (Doc nr.: UM2091, GD2084).

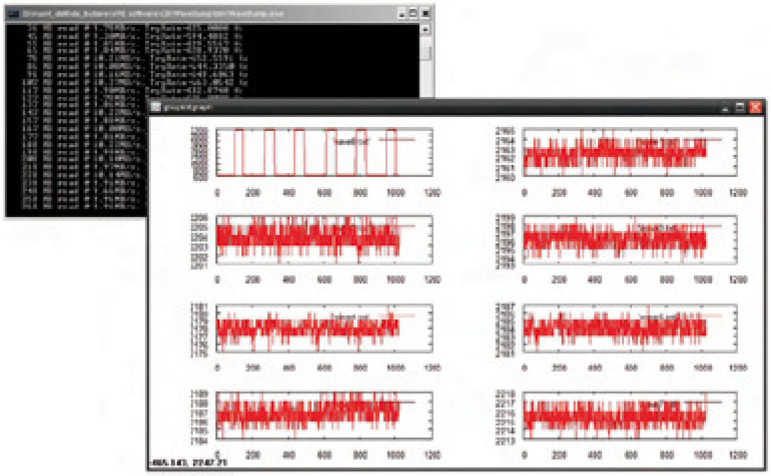


Fig. 4.2: WaveDump output waveforms

- **CAENScope** is a fully graphical program that implements a simple oscilloscope: it allows to see the waveforms, set the trigger thresholds, change the scales of time and amplitude, perform simple mathematical operations between the channels, save data to file and other operations. CAENscope is provided as an executable file; the source codes are not distributed. **NOTE:** CAENScope does not work with digitizers running DPP firmware and it is not compliant with x742 digitizer family. For more details please see the CAENScope Quick Start Guide GD2484.

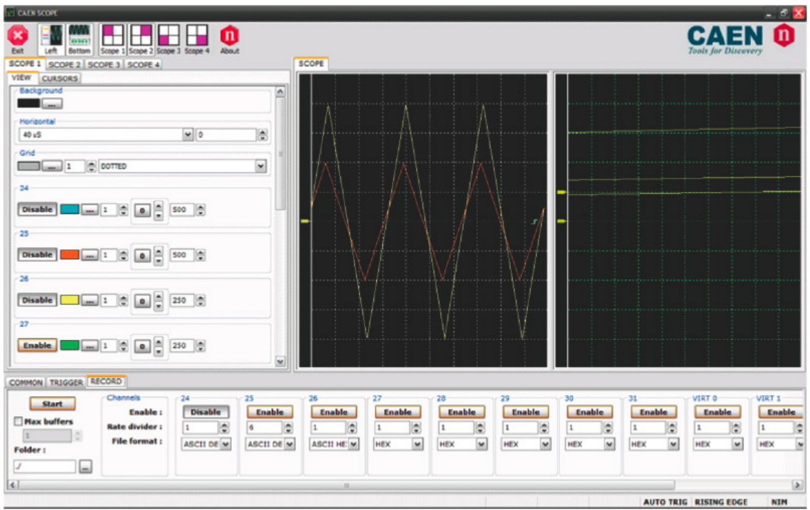


Fig. 4.3: CAENScope oscilloscope tab

- **CAENUpgrader** is a software composed of command line tools together with a Java Graphical User Interface (for Windows and Linux OS). CAENUpgrader allows in few easy steps to upload different firmware versions on CAEN boards, to upgrade the

VME digitizers PLL, to get board information and to manage the firmware license. CAENUpgrader requires the installation of 2 CAEN libraries (CAENComm, CAENVMELib) and Java SE6 (or later). CAENComm allows CAENUpgrader to access target boards via USB or via CAEN proprietary CONET optical link.

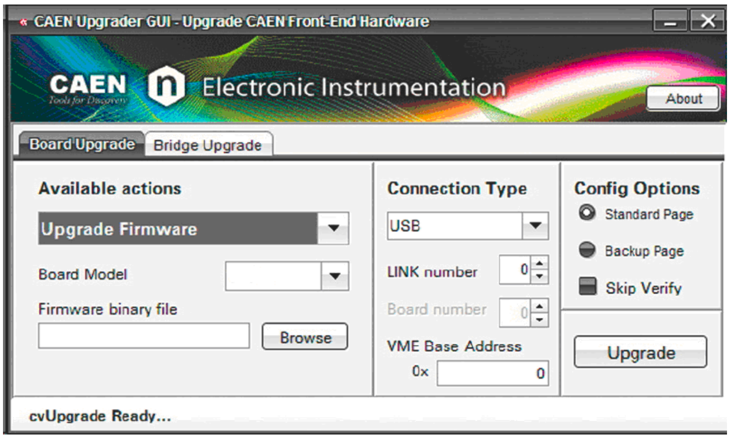


Fig. 4.4: CAENUpgrader Graphical User Interface

- **DPP Control Software** is an application that manages the acquisition in the digitizers which have DPP firmware installed on it. The program is made of different parts: there is a GUI whose purpose is to set all the parameters for the DPP and for the acquisition; the GUI generates a textual configuration file that contains all the parameters. This file is read by the Acquisition Engine (**DPPrunner)**, which is a C console application that programs the digitizer according to the parameters, starts the acquisition and manage the data readout. The data, that can be waveforms, time stamps, energies or other quantities of interest, can be saved to output files or plotted using gnuplot as an external plotting tool, exactly like in WaveDump. NOTE: so far DPP Control Software is developed for Mod. x724 and Mod. x720 digitizer series.

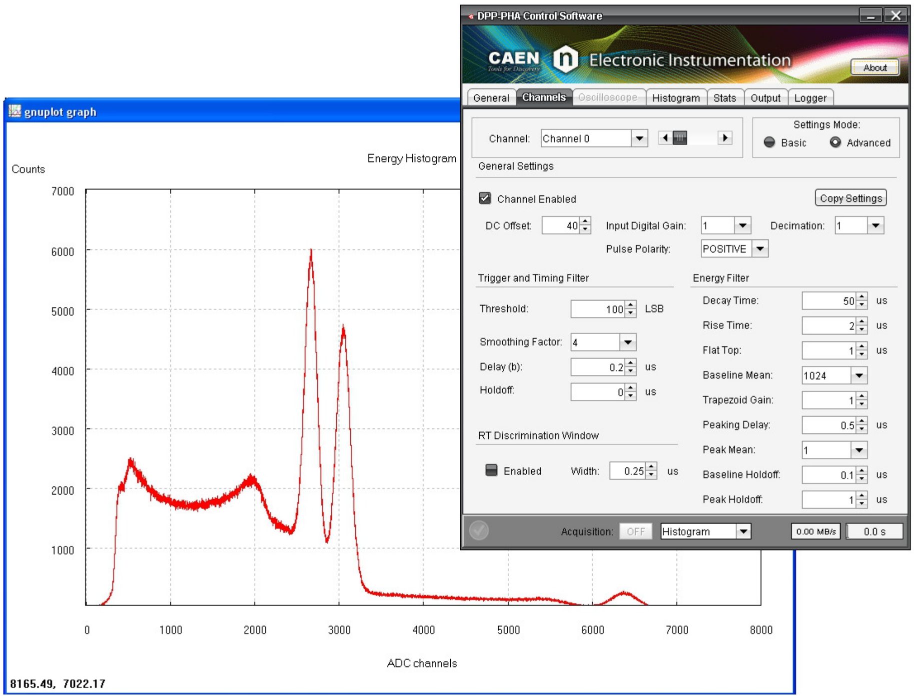


Fig. 4.5: DPP Control Software Graphical User Interface and Energy plot

5. VME Interface

The following sections will describe in detail the board's VME-accessible registers content.

⚠ N.B.: bit fields that are not described in the register bit map are reserved and must not be over written by the User.

5.1. Registers address map

Table 5.1: Address Map for the Model V1751

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	A24/A32/A64	D32	R	X	X	X
Channel n THRESHOLD	0x1n80	A24/A32	D32	R/W	X	X	
Channel n STATUS	0x1n88	A24/A32	D32	R	X	X	
Channel n AMC FPGA FIRMWARE REVISION	0x1n8C	A24/A32	D32	R			
Channel n BUFFER OCCUPANCY	0x1n94	A24/A32	D32	R	X	X	X
Channel n DAC	0x1n98	A24/A32	D32	R/W	X	X	
Channel n ADC CONFIGURATION	0x1n9C	A24/A32	D32	R	X	X	
Channel n TEMPERATURE MONITOR	0x1nA8	A24/A32	D32	R	X	X	X
CHANNEL CONFIGURATION	0x8000	A24/A32	D32	R/W	X	X	
CHANNEL CONFIGURATION BIT SET	0x8004	A24/A32	D32	W	X	X	
CHANNEL CONFIGURATION BIT CLEAR	0x8008	A24/A32	D32	W	X	X	
BUFFER ORGANIZATION	0x800C	A24/A32	D32	R/W	X	X	
BUFFER FREE	0x8010	A24/A32	D32	R/W			
CUSTOM SIZE	0x8020	A24/A32	D32	R/W	X	X	
BROADCAST ADC CONFIGURATION	0x809C	A24/A32	D32	R/W	X	X	
ACQUISITION CONTROL	0x8100	A24/A32	D32	R/W	X	X	
ACQUISITION STATUS	0x8104	A24/A32	D32	R			
SW TRIGGER	0x8108	A24/A32	D32	W			
TRIGGER SOURCE ENABLE MASK	0x810C	A24/A32	D32	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	A24/A32	D32	R/W	X	X	
POST TRIGGER SETTING	0x8114	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O DATA	0x8118	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	A24/A32	D32	R/W	X	X	
CHANNEL ENABLE MASK	0x8120	A24/A32	D32	R/W	X	X	
ROC FPGA FIRMWARE REVISION	0x8124	A24/A32	D32	R			
EVENT STORED	0x812C	A24/A32	D32	R	X	X	X
SET MONITOR DAC	0x8138	A24/A32	D32	R/W	X	X	
SW ADC SYNC	0x813C	A24/A32	D32	W			
BOARD INFO	0x8140	A24/A32	D32	R			
MONITOR MODE	0x8144	A24/A32	D32	R/W	X	X	
EVENT SIZE	0x814C	A24/A32	D32	R	X	X	X
VME CONTROL	0xEF00	A24/A32	D32	R/W	X		
VME STATUS	0xEF04	A24/A32	D32	R			
BOARD ID	0xEF08	A24/A32	D32	R/W	X	X	
MULTICAST BASE ADDRESS & CONTROL	0xEF0C	A24/A32	D32	R/W	X		
RELOCATION ADDRESS	0xEF10	A24/A32	D32	R/W	X		
INTERRUPT STATUS ID	0xEF14	A24/A32	D32	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	A24/A32	D32	R/W	X	X	

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
BLT EVENT NUMBER	0xEF1C	A24/A32	D32	R/W	X	X	
SCRATCH	0xEF20	A24/A32	D32	R/W	X	X	
SW RESET	0xEF24	A24/A32	D32	W			
SW CLEAR	0xEF28	A24/A32	D32	W			
FLASH ENABLE	0xEF2C	A24/A32	D32	R/W	X		
FLASH DATA	0xEF30	A24/A32	D32	R/W	X		
CONFIGURATION RELOAD	0xEF34	A24/A32	D32	W			
CONFIGURATION ROM	0xF000-0xF3FC	A24/A32	D32	R			

5.2. Configuration ROM (0xF000-0xF084; r)

The following registers contain some module's information, they are D32 accessible (read only):

- **OUI**: manufacturer identifier (IEEE OUI)
- **Version**: purchased version
- **Board ID**: Board identifier
- **Revision**: hardware revision identifier
- **Serial MSB**: serial number (MSB)
- **Serial LSB**: serial number (LSB)

Table 5.2: ROM Address Map for the Model V1751

Description	Address	Content
checksum	0xF000	*0xA4*
checksum_length2	0xF004	0x00
checksum_length1	0xF008	0x00
checksum_length0	0xF00C	0x20
constant2	0xF010	0x83
constant1	0xF014	0x84
constant0	0xF018	0x01
c_code	0xF01C	0x43
r_code	0xF020	0x52
oui2	0xF024	0x00
oui1	0xF028	0x40
oui0	0xF02C	0xE6
vers	0xF030	V1751, VX1751: 0x60; V1751B, VX1751B: 0x61 V1751C, VX1751C: 0x62
board2	0xF034	V1751-B-C: 0x00 ; VX1751-B-C: 0x01
board1	0xF038	0x06
board0	0xF03C	0xD7
revis3	0xF040	*0x00*
revis2	0xF044	*0x00*
revis1	0xF048	*0x00*
revis0	0xF04C	*0x01*
sernum1	0xF080	*0x00*
sernum0	0xF084	*0x16*

These data are written into one Flash page; at Power ON the Flash content is loaded into the Configuration RAM, where it is available for readout.

5.3. Channel n Threshold (0x1n80; r/w)

Bit	Function

[9:0]	Threshold Value for Trigger Generation

Each channel can generate a local trigger as the digitized signal exceeds the Vth threshold. This register allows to set Vth (LSB=input range/10bit); see also § 3.4.3.

5.4. Channel n Status (0x1n88; r)

Bit	Function
[8]	Over temperature flag 0 = Ch temperature OK 1 = Ch Over temperature
[7]	Power down flag 0 = Ch Power OK 1 = Ch Power Down
[6]	Calibrating: 1 = calibration done 0 = calibration in progress
[5]	Buffer free error: 1 = trying to free a number of buffers too large
[3,4]	reserved
[2]	Channel n DAC Channel n DAC / ADC bus Busy (see § 5.7) 1 = Busy 0 = Ready
[1]	Memory empty
[0]	Memory full

5.5. Channel n AMC FPGA Firmware (0x1n8C; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).
Example: revision 1.3 of 12th June 2007 is: 0x76120103

5.6. Channel n Buffer Occupancy (0x1n94; r)

Bit	Function
[10:0]	Occupied buffers (0..1024)

5.7. Channel n DAC (0x1n98; r/w)

Bit	Function
[15:0]	DAC Data

Bits [15:0] allow to define a DC offset to be added the input signal in the ±0.5V range, see also § 3.1.1. When Channel n Status bit 2 is set to 0, DC offset is updated (see § 5.4).

5.8. Channel n ADC Configuration (0x1n9C; w)

Bit	Function
[1]	Calibration
[0]	Power Down configuration 0 = Ch Power OK 1 = Ch Power Down

This register allows to pilot the relevant ADC signal.

5.9. Channel n Temperature Monitor (0x1nA8; r)

Bit	Function
[7:0]	Monitored Temperature (℃)

These registers allow to monitor the temperature of ADC chips; since each ADC houses two channels (0-1, 2-3. 4-5, 6-7) these registers provide identical values in pairs.

5.10. Channel Configuration (0x8000; r/w)

Bit	Function
[12]	0 = 1 GS/s rate 1 = 2 GS/s rate (D*ual Edge Sampling*) When Dual Edge Sampling mode is used, make sure that the EVEN channels are disconnected
[11:7]	reserved
[6]	0 = Trigger Output on Input Over Threshold 1 = Trigger Output on Input Under Threshold allows to generate local trigger either on channel over or under threshold (see § 5.3)
[5]	reserved
[4]	0 = Memory Random Access 1 = Memory Sequential Access
[3]	0 = Test Pattern Generation Disabled 1 = Test Pattern Generation Enabled
[2]	reserved
[1]	0 = Trigger Overlapping Not Enabled 1 = Trigger Overlapping Enabled Allows to handle trigger overlap (see § 3.3.3)
[0]	reserved

This register allows to perform settings which apply to all channels. It is possible to perform selective set/clear of the Channel Configuration register bits writing to 1 the corresponding set and clear bit at address 0x8004 (set) or 0x8008 (clear) see the following § 5.11 and 5.12. Default value is 0x10.

5.11. Channel Configuration Bit Set (0x8004; w)

Bit	Function
[12:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 1.

5.12. Channel Configuration Bit Clear (0x8008; w)

Bit	Function
[12:0]	Bits set to 1 means that the corresponding bits in the Channel Configuration register are set to 0.

5.13. Buffer Organization (0x800C; r/w)

Bit	Function
[3:0]	BUFFER CODE

The BUFFER CODE allows to divide the available Output Buffer Memory into a certain number of blocks, according to the following table:

Table 5.3: Output Buffer Memory block division (case of 1.8Msamples/ch memory)

CODE	Nr. of blocks	Block_size @1GS/s	Samples/block @1GS/s	Block_size @2GS/s	Samples/block @2GS/s
0000	1	1.835M	1.835M	3.706M	3.706M
0001	2	0.926M	0.926M	1.835M	1.835M
0010	4	...	…	...	...
0011	8				
0100	16				
0101	32				
0110	64				
0111	128				
1000	256				
1001	512				
1010	1024				

A write access to this register causes a Software Clear, see § 3.8. This register must not be written while acquisition is running. The number of Samples/block depends on Custom size register setting (see § 5.15)

5.14. Buffer Free (0x8010; r/w)

Bit	Function
[11:0]	N = Frees the first N Output Buffer Memory Blocks, see § 5.13

5.15. Custom Size (0x8020; r/w)

Bit	Function
[31:0]	0= Custom Size disabled N_{LOC} ($\neq$0) = Number of memory locations per event (1 location = 7 samples @ 1GS/s; 14 samples @ 2GS/s)

This register must not be written while acquisition is running.

5.16. Broadcast ADC Configuration (0x809C; w)

Bit	Function
[1]	Calibration
[0]	Power Down; must always be 0

This register allows to pilot all the relevant ADC signal.

5.17. Acquisition Control (0x8100; r/w)

Bit	Function
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers (see § 3.3.3)
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[1:0]	00 = REGISTER-CONTROLLED RUN MODE 01 = S-IN CONTROLLED RUN MODE 10 = reserved 11 = MULTI-BOARD SYNC MODE

Bit [2] allows to Run and Stop data acquisition; when such bit is set to 1 the board enters Run mode and a Memory Reset (see § 3.8.2) is automatically performed. When bit [2] is reset to 0 the stored data are kept available for readout. In Stop Mode all triggers are neglected.

Bits [1:0] description:
00 = REGISTER-CONTROLLED RUN MODE: multiboard synchronization via S_IN front panel signal
– RUN control: start/stop via set/clear of bit[2]
– GATE always active (Continuous Gate Mode)
01 = S-IN CONTROLLED RUN MODE: Multiboard synchronization via S-IN front panel signal
– S-IN works both as SYNC and RUN_START command
– GATE always active (Continuous Gate Mode)
11 = MULTI-BOARD SYNC MODE
– Used only for Multiboard synchronization

5.18. Acquisition Status (0x8104; r)

Bit	Function
[8]	Board ready for acquisition (PLL and ADCs are synchronized correctly) 0 = not ready 1 = ready This bit should be checked after software reset to ensure that the board will enter immediately run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Status Flag (see § 2.5.1): 0 = PLL loss of lock 1 = no PLL loss of lock NOTE: This bit acts as a flag, indicating that a PLL unlock condition has occurred from the last register read. This bit is internally restored to 1 after a read access to Status Register (see § 5.34)
[6]	PLL Bypass mode (see § 2.5.1): 0 = No bypass mode 1 = Bypass mode
[5]	Clock source (see § 2.6): 0 = Internal 1 = External
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	0 = RUN off 1 = RUN on
[1,0]	reserved

5.19. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access to this location generates a trigger via software

5.20. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:27]	reserved
[26:24]	Local trigger coincidence level (default = 0)
[23:8]	reserved
[7]	0 = Channel 7 trigger disabled 1 = Channel 7 trigger enabled
[6]	0 = Channel 6 trigger disabled 1 = Channel 6 trigger enabled
[5]	0 = Channel 5 trigger disabled 1 = Channel 5 trigger enabled
[4]	0 = Channel 4 trigger disabled 1 = Channel 4 trigger enabled
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled 1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,7] enable the channels to generate a local trigger as the digitized signal exceeds the Vth threshold (see § 3.4.3). Bit0 enables Ch0 to generate the trigger, bit1 enables Ch1 to generate the trigger and so on.
Bits [26:24] allows to set minimum number of channels that must be over threshold, beyond the triggering channel, in order to actually generate the local trigger signal; for example if bit[7:0]=FF (all channels enabled) and Local trigger coincidence level = 1, whenever one channel exceeds the threshold, the trigger will be generated only if at least another channel is over threshold at that moment. Local trigger coincidence level must be smaller than the number of channels enabled via bit[7:0] mask.
EXTERNAL TRIGGER ENABLE (bit30) enables the board to sense TRG-IN signals
SW TRIGGER ENABLE (bit 31) enables the board to sense software trigger (see § 5.19).

5.21. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:8]	reserved
[7]	0 = Channel 7 trigger disabled 1 = Channel 7 trigger enabled
[6]	0 = Channel 6 trigger disabled 1 = Channel 6 trigger enabled
[5]	0 = Channel 5 trigger disabled 1 = Channel 5 trigger enabled
[4]	0 = Channel 4 trigger disabled 1 = Channel 4 trigger enabled
[3]	0 = Channel 3 trigger disabled 1 = Channel 3 trigger enabled
[2]	0 = Channel 2 trigger disabled

Bit	Function
	1 = Channel 2 trigger enabled
[1]	0 = Channel 1 trigger disabled 1 = Channel 1 trigger enabled
[0]	0 = Channel 0 trigger disabled 1 = Channel 0 trigger enabled

This register bits[0,7] enable the channels to generate a TRG_OUT front panel signal as the digitized signal exceeds the Vth threshold (see § 3.4.3).
Bit0 enables Ch0 to generate the TRG_OUT, bit1 enables Ch1 to generate the TRG_OUT and so on.
EXTERNAL TRIGGER ENABLE (bit30) enables the board to generate the TRG_OUT
SW TRIGGER ENABLE (bit 31) enables the board to generate TRG_OUT (see § 5.19).

5.22. Post Trigger Setting (0x8114; r/w)

Bit	Function
[31:0]	Post trigger value

The register value sets the number of post trigger samples. The number of post trigger samples is
$N_S=[(N_{PV} + N_{DEL}) \cdot 16 \pm 15]$
This formula becomes $N_S= 2 \cdot [(N_{PV} + N_{DEL}) \cdot 16 \pm 15]$ in DES mode
N_S = number of post trigger samples.
N_{PV} = PostTriggerValue = Content of this register.
N_{DEL} = ConstantLatency = constant number of samples added due to the latency associated to the trigger processing logic in the ROC FPGA; N_{DEL} is 4 with external trigger and 8 with internal trigger.

5.23. Front Panel I/O Data (0x8118; r/w)

Bit	Function
[15:0]	Front Panel I/O Data

Allows to Readout the logic level of LVDS I/Os and set the logic level of LVDS Outputs.

5.24. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[15]	0 = I/O Normal operations: TRG-OUT signals outside trigger presence (trigger are generated according to Front Panel Trigger Out Enable Mask setting, see § 5.21) 1= I/O Test Mode: TRG-OUT is a logic level set via bit 14
[14]	1= TRG-OUT Test Mode set to 1 0 = TRG-OUT Test Mode set to 0
[13:10]	*reserved*
[9]	PATTERN_LATCH_MODE = 0: PATTERN field into event headers is the status of 16 LVDS Front Panel Inputs latched with board internal trigger (if a post trigger value is set, the internal trigger is delayed respect to external one). = 1: PATTERN field into event headers is the status of 16 LVDS Front Panel Inputs latched with external trigger rising edge.
[8]	*reserved*
[7:6]	00 = General Purpose I/O 01 = Programmed I/O 10 = Pattern mode: LVDS signals are input and their value is written into header PATTERN field (see § 3.3.4)
[5]	0 = LVDS I/O 15..12 are inputs

Bit	Function
	1 = LVDS I/O 15..12 are outputs
[4]	0 = LVDS I/O 11..8 are inputs 1 = LVDS I/O 11..8 are outputs
[3]	0 = LVDS I/O 7..4 are inputs 1 = LVDS I/O 7..4 are outputs
[2]	0 = LVDS I/O 3..0 are inputs 1 = LVDS I/O 3..0 are outputs
[1]	0= panel output signals (TRG-OUT/CLKOUT) enabled 1= panel output signals (TRG-OUT/CLKOUT) enabled in high impedance
[0]	0 = TRG/CLK are NIM I/O Levels 1 = TRG/CLK are TTL I/O Levels

Bits [5:2] are meaningful for General Purpose I/O use only

5.25. Channel Enable Mask (0x8120; r/w)

Bit	Function
[7]	0 = Channel 7 disabled 1 = Channel 7 enabled
[6]	0 = Channel 6 disabled 1 = Channel 6 enabled
[5]	0 = Channel 5 disabled 1 = Channel 5 enabled
[4]	0 = Channel 4 disabled 1 = Channel 4 enabled
[3]	0 = Channel 3 disabled 1 = Channel 3 enabled
[2]	0 = Channel 2 disabled 1 = Channel 2 enabled
[1]	0 = Channel 1 disabled 1 = Channel 1 enabled
[0]	0 = Channel 0 disabled 1 = Channel 0 enabled

Enabled channels provide the samples which are stored into the events (and not erased). The mask cannot be changed while acquisition is running. When Dual Edge Sampling mode is used, make sure that the EVEN channels are disconnected and disable EVEN channels (0, 2, 4, 6) through this register.

5.26. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

5.27. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

This register value cannot exceed the maximum number of available buffers according to setting of buffer size register.

5.28. Set Monitor DAC (0x8138; r/w)

Bit	Function
[11:0]	This register allows to set the DAC value (12bit)

This register allows to set the DAC value in Voltage level mode (see § 2.7). LSB = 0.244 mV, terminated on 50 Ohm.

5.29. SW ADC SYNC (0x813C; r/w)

Bit	Function
[31:0]	This register allows to ensure the proper ADC synchronization within the board channels after a calibration procedure

5.30. Board Info (0x8140; r)

Bit	Function
[15:8]	Memory size code (V1751-V1751B: 0x02); (V1751C: 0x10)
[7:0]	Board Type (0x05)

5.31. Monitor Mode (0x8144; r/w)

Bit	Function
[2:0]	This register allows to encode the Analog Monitor (see § 3.6) operation: 000 = majority 001 = waveform generator (saw tooth) 010 = *reserved* 011 = buffer occupancy 100 = voltage level

5.32. Event Size (0x814C; r)

Bit	Function
[31:0]	Nr. of 32 bit words in the next event

5.33. VME Control (0xEF00; r/w)

Bit	Function
[7]	0 = Release On Register Access (RORA) Interrupt mode (default) 1 = Release On AcKnowledge (ROAK) Interrupt mode
[6]	0 = RELOC Disabled (BA is selected via Rotary Switch; see § 2.6) 1 = RELOC Enabled (BA is selected via RELOC register; see § 5.37)
[5]	0 = ALIGN64 Disabled 1 = ALIGN64 Enabled (see § 3.11.1.2)
[4]	0 = BERR Not Enabled; the module sends a DTACK signal until the CPU inquires the module 1 = BERR Enabled; the module is enabled either to generate a Bus error to finish a block transfer or during the empty buffer read out in D32
[3]	0 = Optical Link interrupt disabled 1 = Optical Link interrupt enabled
[2 :0]	Interrupt level (0= interrupt disabled)

Bit [7]: this setting is valid only for interrupts broadcasted on VMEbus; interrupts broadcasted on optical link feature RORA mode only.

– In RORA mode, interrupt request can be removed by accessing VME Control register (see § 5.33) and disabling the active interrupt level.

– In ROAK mode, interrupt request is automatically removed via an interrupt acknowledge cycle. Interrupt generation is restored by setting an Interrupt level > 0 via VME Control register.

5.34. VME Status (0xEF04; r)

Bit	Function
[2]	0 = BERR FLAG: no Bus Error has occurred 1 = BERR FLAG: a Bus Error has occurred (this bit is re-set after a status register read out)
[1]	0 = The Output Buffer is not FULL; 1 = The Output Buffer is FULL.
[0]	0 = No Data Ready; 1 = Event Ready

5.35. Board ID (0xEF08; r/w)

Bit	Function
[4 :0]	GEO

– VME64X versions: this register can be accessed in read mode only and contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the EVENT HEADER Board ID field (see § 3.3.4).
– Other versions: this register can be accessed both in read and write mode; it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the EVENT HEADER Board ID field (see § 3.3.4)

5.36. MCST Base Address and Control (0xEF0C; r/w)

Bit	Function
[9:8]	Allows to set up the board for daisy chaining: 00 = disabled board 01 = last board 10 = first board 11 = intermediate
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.

5.37. Relocation Address (0xEF10; r/w)

Bit	Function
[15:0]	These bits contains the A31...A16 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module.

5.38. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31:0]	This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle

5.39. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[9:0]	INTERRUPT EVENT NUMBER

If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER

5.40. BLT Event Number (0xEF1C; r/w)

Bit	Function
[7:0]	This register contains the number of complete events which has to be transferred via BLT/CBLT (see § 3.11.1.2).

5.41. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (*to be used to write/read words for VME test purposes*)

5.42. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this location allows to perform a software reset

5.43. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this location clears all the memories

5.44. Flash Enable (0xEF2C; r/w)

Bit	Function
[0]	0 = Flash write ENABLED 1 = Flash write DISABLED

This register is handled by the Firmware upgrade tool.

5.45. Flash Data (0xEF30; r/w)

Bit	Function
[7:0]	Data to be serialized towards the SPI On board Flash

This register is handled by the Firmware upgrade tool.

5.46. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register causes a software reset (see § 3.8), a reload of Configuration ROM parameters and a PLL reconfiguration.

6. Installation

- The Mod. V1751 fits into 6U VME crates.
- **The V1751 cannot be operated with CAEN crates VME8001/8002**
- VX1751 versions require VME64X compliant crates
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DAMAGE THE MODULE!

CAUTION

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

6.1. Power ON sequence

To power ON the board follow this procedure:

1. insert the V1751 board into the crate
2. power up the crate

6.2. Power ON status

At power ON the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration (see § 5)

6.3. Firmware upgrade

The board can store two firmware versions, called STD and BKP respectively; at Power On, a microcontroller reads the Flash Memory and programs the module with the firmware version selected via the JP2 jumper (see § 2.6), which can be placed either on the STD position (left), or in the BKP position (right). It is possible to upgrade the board firmware via VME, by writing the Flash with CAENUpgrader software (see § 4) available at www.caen.it website. Please refer to CAENUpgrader QuickStart Guide about instructions for use.

It is strongly suggested to upgrade ONLY one of the stored firmware revisions (generally the STD one): if both revision are simultaneously updated, and a failure occurs, it will not be possible to upload the firmware via VME again!

6.3.1. V1751 Upgrade files description

The board hosts one FPGA on the mainboard and one FPGA for each of the eight channels. The channel FPGAs firmware is identical. A unique file is provided that will updated all the FPGA at the same time.

ROC FPGA MAINBOARD FPGA (Readout Controller + VME interface)

There is one FPGA Altera Cyclone EP1C20.

AMC FPGA CHANNEL FPGA (ADC readout/Memory Controller):

There is one FPGA Altera Cyclone EP1C4

All FPGAs can be upgraded via VMEBUS;

CAENUpgrader utility program must be used for this purpose.

The programming file has the extension .CFA (CAEN Firmware Archive) and is a sort of archive format file aggregating all the standard firmware files compatible with the same family of digitizers.

CFA and its name follows this general scheme:

x751_revX.Y_W.Z.CFA

where:

- x751 are all the boards the file is compliant to: DT5751, N6751, V1751
- X.Y is the major/minor revision number of the mainboard FPGA
- W.Z is the major/minor revision number of the channel FPGA

WARNING: you can restore the previous FW revision in case there is a failure when you run the upgrading program. There is a jumper on the mainboard that allows to select the "backup" copy of the firmware. You must upgrade all the FPGAs and keep the revisions aligned; it is not guaranteed that the latest revision of one FPGA is compatible with an older revision.